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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/212,291	12/16/1998	CHINNA PRUDVI	2207/5915	8642

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EXAMINER
THAI, TUAN V

ART UNIT	PAPER NUMBER
2186	18

DATE MAILED: 07/02/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

PRG

Office Action Summary	Application No.	Applicant(s)	
	09/212,291	PRUDVI ET AL.	
	Examiner	Art Unit	
	Tuan V. Thai	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 February 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *25 February 2002* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

PART III

RESPONSE TO AMENDMENTS

1. This action is responsive to communication filed on February 25, 2002. This amendment has been entered and carefully considered. Claims 1-29 are again presented for examination. Claims 24-29 are newly added.

2. The objection of Drawing 1 is withdrawn due to amendment filed February 25, 2002.

3. The rejection of claims 6 and 7 under 35 USC 112 second paragraph is withdrawn due to amendment filed February 25, 2002.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 8-10, 22, 24 and 29 are rejected under 35 U.S.C. 102(b) as being anticipated by Sachs et al. (USPN:

4,884,197) (hereinafter Sachs).

As per claim 8, Sachs teaches the invention as claimed including a processing agent comprising a transaction queue as being equivalent to the TLB 350 having a plurality of queue entries (lines) (e.g. see column 22, line 49 et seq.), wherein the queue entries further comprising a primary sub entry including an address information and status information provided for a first external transaction, and a secondary subentry provided including a status portion provided for a second external transaction is explicitly taught by Sachs as each line having virtual address field VA for storing address information and a reference bit R field or a dirty bit D field for storing status information of the first external transaction being read/write transactions (with respect to the status for the second external transaction, note also an user valid bit UV field, a supervisor valid bit field, a protection level word PL field and a system tag ST field; e.g. see column 22, lines 59 et seq.; column 24, lines 27 et seq.); wherein the first and second external transactions relate to the same address portion is taught by Sachs; for example, as pointed out by Examiner, the status portion for the primary sub entry is taught as the R status field or D status field to indicate whether the TLB line/page has been referenced/accessed to by a read or write access; knowingly, for another read/write transaction (second

external transaction) to the same address portion/line or page; the dirty bit D field is set in accordance; at the same time, the supervisor valid field bit (SV) or user valid field bit (UV) is set to ONE depending upon the mode at the time (e.g. column 24, lines 45 et seq.);

As per claim 9, wherein the status portion of the primary entry includes a field representing whether the first transaction is part of a multiple transaction queue is equivalently taught by Sachs as the reference bit R or the dirty bit D field of each line indicating that the line has been referenced by a read or write transaction (multiple transaction sequence), or having been modified by a write transactions (e.g. see column 22, lines 59 et seq.; column 24, lines 27 et seq.);

As per claim 10, Sachs discloses the TLB control logic unit 820 as being equivalent to the control logic being claimed, coupling to the TLB 350 for cycle through the queue entries and post transaction therefrom (e.g. see figure 23);

As per claim 22, see argument with respect to claim 8.

As per claim 24, Sachs teaches the invention as claimed including a processing agent (e.g. see figures 8 and 9), the agent comprising an cache memory 320 having a plurality of cache lines; for example, Sachs discloses that the cache memory 320 having three fields, a used bit field, and two identical read-write memory fields W and X wherein each field W and X contain

multiple lines, and each line in the cache contains multiple entries (fields) (e.g. see figure 10.B) and having tag field RA, line valid bit LV, line dirty bit LD and multiple data entries DT (e.g. see column 22, lines 14 et seq.); Sachs further discloses that the cache entries include a tag portion for storing address information as being the real address field RA (e.g. see figure 10B, and column 22, lines 32 et seq.); wherein the processing agent posts a series of external transactions related to the address information, each of the external transactions filling one of the cache entries in the cache lines is taught by Sachs as when the requested information for the addressed location is not stored in the respective cache-MMU memories (cache misses); the micro engine of the cache-MMUs provides a translated physical address for output to the main memory 140, the corresponding information is thereafter transferred from main memory to the respective instruction cache-MMU or to/from the cache-MMU and as needed to the processor 110 (e.g. see column 6, lines 13-21);

As per claim 29, wherein data line corresponds to the maximum amount of data that can be transferred in a single bus transaction is taught by Sachs to the extent that it is being claimed; for example, when detailing data cache bus, Sachs discloses on store operations, the CPU puts an address following by data on the address/data bus for one (single) clock/bus cycle (e.g. see column 6, lines 27 et seq.);

6. Claims 17-21, 23 and 27-28 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Sachs (USPN: 4,884,197), and being anticipated by Scales et al. (USPN: 4,914,573) (hereinafter Scales).

As per claims 17 and 18, Scales discloses the invention as claimed including a method of processing a data request within a processing agent comprising posting the data request internally within the agent, determining whether the cache hit by comparing address information of the data request with tags stored in the internal cache, and if cache miss occurs, posting a sequence of external transactions to fill a cache line with data associated with the data request (e.g. see column 1, lines 12-32); wherein each cache line is sized to store multiple data line lengths of data is taught by Scales since Scales clearly teaches the cache line supports multiple entries having different size (***If the size of the entries in the cache line is different***) (e.g. see column 7, lines 59-62);

As per claim 19; reading the cache coherency state information associated with the requested data when address information matches a stored tag, and identifying cache miss when coherency information is invalid is embedded in Scales's system and being taught to the extent that it is claimed, since Scales discloses in a conventional system the cache are arranged

as a plurality of lines, each containing plurality of entries which share a common "tag address", ***and a corresponding number of valid bits which when set indicate the validity of the respective entries in the particular cache line*** (e.g. see Scales's column 1, lines 12-17);

As per claims 20 and 21; Scales teaches the determining whether the request hits a tag stored in the cache by comparing the requested data address information with a tag address and generating a single transaction to read the requested data into the agent (e.g. see column 1, lines 19-21;);

As per claim 23, Scales discloses the invention as claimed including a method of processing a data request within a processing agent comprising posting the data request internally within the agent, determining whether the request hit in the cache, when cache miss occurs, posting a series of external transaction to fill a cache line with data associated with the data request (e.g. see column 1, lines 12-32); the external transactions directed to a data-line sized data item identified by an address of the data request and to at least one other data-line-sized item adjacent to the first data item (e.g. see column 2, lines 55-66).

As per claims 27 and 28, wherein data line corresponds to the maximum amount of data that can be transferred in a single bus transaction is taught by Sachs to the extent that it is being

claimed; for example, when detailing data cache bus, Sachs discloses on store operations, the CPU puts an address following by data on the address/data bus for one (single) clock/bus cycle (e.g. see column 6, lines 27 et seq.);

Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-7, 11-16 and 25-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sachs et al. (USPN: 4,884,197); hereinafter Sachs, in view of Scales, III et al., (USPN: 4,914,573) (hereinafter Scales).

As per claim 1, Sachs teaches the invention as claimed including a processing agent (e.g. see figures 8 and 9) to transfer data of predetermined data length in an external transaction, the agent comprising an cache memory 320 having a plurality of cache entries; for example, Sachs discloses that the cache memory 320 having three fields, a used bit field, and two identical read-write memory fields W and X wherein each field W and X contain multiple lines, and each line in the cache contains

multiple entries (fields) (e.g. see figure 10.B) and having tag field RA, line valid bit LV, line dirty bit LD and multiple data entries DT (e.g. see column 22, lines 14 et seq.). Sachs discloses the invention as claimed; however Sachs does not particularly teach that each entry sized to store multiple data line lengths of data. Scales, in his teaching of bus master which selectively attempts to fill complete entries in a cache line, disclose the missing element that known to be required in Sachs in order to arrive at Applicant's current invention wherein Sachs teaches cache memory 22 having a plurality of cache entries (e.g. see column 2, lines 38 et seq.), each of the cache entries include a tag portion for storing address information RA (e.g. see figure 2, column 2, lines 38 et seq.), cache coherency state field [A3, A2] wherein each entry can be sized to store multiple data line lengths of data (e.g. see column 7, lines 59 et seq.). Accordingly, it would have been obvious to one having ordinary skill in the art at the time the current invention was made to implement the cache having multiple cache lines comprising multiple entries, wherein each entry sized to store multiple data line lengths of data as being taught by Scales for that of Sachs. In doing so, it would increase the flexibility of Sachs system by allowing it to serve a broader range of applications and their variants thereby broadening one's potential market and saving investment capital.

As per claim 2, Sachs clearly discloses that the cache entries include a tag portion for storing address information as being the real address field RA (e.g. see figure 10B, and column 22, lines 32 et seq.);

As per claim 3, the match detection logic for the tag portions and control logic provided in communication with the match detection logic is taught by Sachs as the comparators 332 and 334, and the multiplexer 341 (e.g. see figure 9, column 21, lines 4 et seq.; for example, Sachs discloses the match/no match signals output from comparators 332 and 334 indicate a cache hit when the requested real address was presented in the cache and the data was valid, or a cache miss when the requested data is not present in the cache (e.g. see column 21, lines 20 et seq.);

As per claim 4, Sachs clearly teaches each cache line further have a cache coherency state field such that: a cache line valid bit LV, a line dirty bit DT (e.g. see figure 10B, column 22, lines 28 et seq.);

As per claim 5, Sachs discloses his processing agent further comprising a transaction queue as being equivalent to the TLB 350 having a plurality of queue entries (lines) (e.g. see column 22, line 54 et seq.), wherein the queue entries including a primary entry for storing address information and status information of a first external transaction, and a secondary entry for storing status information of a second external transaction is explicitly

taught by Sachs as each line having virtual address field VA for storing address information and a reference bit R field or a dirty bit D field for storing status information of an external transaction being read/write transactions (note also an user valid bit UV field, a supervisor valid bit field, a protection level word PL field and a system tag ST field; e.g. see column 22, lines 59 et seq.; column 24, lines 27 et seq.);

As per claim 6, wherein the status information of the first external transaction includes a field (e.g. the reference bit R or the dirty bit D) indicating that the line has been referenced by a read or write transaction (multiple transaction sequence), or having been modified by a write transactions (e.g. see column 22, lines 59 et seq.; column 24, lines 27 et seq.);

As per claim 7, Sachs discloses the invention as claimed; however Sachs does not particularly teach that the total number of primary and secondary entries equals to the number of data line lengths provided in the cache entries. First of all, it should be noted that the total number of lines in both cache and TLB being disclosed in Sachs's system is a system dependent feature, it can be varied dependent on what system they are implemented within. Secondly, Sachs clearly discloses the W and X memories in BOTH cache memory 320 and TLB 350 each contain multiple lines, and as an example for illustration in the current invention, Sachs selects the number of cache lines being equal to

128 lines (e.g. see column 22, line 22); and the number of lines in the TLB is 64 lines (e.g. see column 22, line 54). Accordingly, it would have been obvious to one having ordinary skill in the art at the time the current invention was made to implement both cache and TLB to have the same number of lines since the numbers of lines in both cache and TLB are changeable as indicated by Sachs. In addition, doing so, it would allow the TLB to buffer more data for reference which results to increasing data hit rate in both TLB and cache, therefore being advantageous.

As per claim 11, Sachs disclose a processing agent (e.g. see figures 8 and 9) comprising an cache memory 320 having a plurality of cache entries; for example, Sachs discloses that the cache memory 320 having three fields, a used bit field, and two identical read-write memory fields W and X wherein each field W and X contain multiple lines, and each line in the cache contains multiple entries (fields) (e.g. see figure 10.B) and having tag field RA, line valid bit LV, line dirty bit LD and multiple data entries DT (e.g. see column 22, lines 14 et seq.). A transaction queue system as being equivalent to the TLB 350 having a plurality of queue entries (lines) to post external transactions, each external transaction related to a single data line (e.g. see column 22, line 54 et seq.), wherein the internal cache and the transaction queue system each receive data requests on a common

input (e.g. see figure 8 show common input line being connected to both TLB 270 and cache 220). Sachs discloses the invention as claimed; however Sachs does not particularly teach that each entry sized to store multiple data line lengths of data. Scales, in his teaching of bus master which selectively attempts to fill complete entries in a cache line, disclose the missing element that known to be required in Sachs in order to arrive at Applicant's current invention wherein Sachs teaches cache memory 22 having a plurality of cache entries (e.g. see column 2, lines 38 et seq.), each of the cache entries include a tag portion for storing address information RA (e.g. see figure 2, column 2, lines 38 et seq.), cache coherency state field [A3, A2] wherein each entry can be sized to store multiple data line lengths of data (e.g. see column 7, lines 59 et seq.). Accordingly, it would have been obvious to one having ordinary skill in the art at the time the current invention was made to implement the cache having multiple cache lines comprising multiple entries, wherein each entry sized to store multiple data line lengths of data as being taught by Scales for that of Sachs. In doing so, it would increase the flexibility of Sachs system by allowing it to serve a broader range of applications and their variants thereby broadening one's potential market and saving investment capital.

As per claim 12, wherein the internal cache and the transaction queue system communicate by signal lines (e.g. see

figure 8);

As per claim 13, wherein the signals line include a cache hit signal line and a tag hit signal line (e.g. see figure 9, column 19, lines 58 et seq.; column 20, lines 4 et seq.);

As per claim 14, Sachs teaches the invention as claimed including a processing agent comprising a transaction queue as being equivalent to the TLB 350 having a plurality of queue entries (lines) (e.g. see column 22, line 54 et seq.), wherein the queue entries further comprising a primary sub entry including an address information and status information provided for a first external transaction, and a secondary subentry provided including a status portion provided for a second external transaction is explicitly taught by Sachs as each line having virtual address field VA for storing address information and a reference bit R field or a dirty bit D field for storing status information of first external transaction being read/write transactions (with respect to status for the second external transaction, note also an user valid bit UV field, a superior valid bit field, a protection level word PL field and a system tag ST field; e.g. see column 22, lines 59 et seq.; column 24, lines 27 et seq.);

As per claim 15, wherein the status portion of the primary entry includes a field representing whether the first transaction is part of a multiple transaction queue is equivalently taught by

Sachs as the reference bit R or the dirty bit D field of each line indicating that the line has been referenced by a read or write transaction (multiple transaction sequence), or having been modified by a write transactions (e.g. see column 22, lines 59 et seq.; column 24, lines 27 et seq.);

As per claim 16, Sachs discloses the TLB control logic unit 820 as being equivalent to the control logic being claimed, coupling to the TLB 350 for cycle through the queue entries and post transaction therefrom (e.g. see figure 23);

As per claims 25 and 26, wherein data line corresponds to the maximum amount of data that can be transferred in a single bus transaction is taught by Sachs to the extent that it is being claimed; for example, when detailing data cache bus, Sachs discloses on store operations, the CPU puts an address following by data on the address/data bus for one (single) clock/bus cycle (e.g. see column 6, lines 27 et seq.);

9. As to the remark, with respect to claims 8-10 and 22; again, Examiner would like to emphasize that different status portions of an external transaction is taught by Sachs as the R status field or D status field to indicate whether the TLB line/page has been referenced/accessed to by a read or write access; note also an user valid bit UV field, a supervisor valid bit field, a protection level word PL field and a system tag ST field; e.g.

see column 22, lines 59 et seq.; column 24, lines 27 et seq.); with respect to the first and second external transactions relate to the same address portion; again, the status portion for the primary sub entry is taught as the R status field or D status field to indicate whether the TLB line/page has been referenced/accessed to by a read or write access; knowingly, for another read/write transaction (second external transaction) to the same address portion/line or page; the dirty bit D field is set in accordance; at the same time, the supervisor valid field bit (SV) or user valid field bit (UV) is set to ONE depending upon the mode at the time (e.g. column 24, lines 45 et seq.). Applicant's counsel further contended that Scales fails to teach or suggest transferring multiple data line lengths of data whenever a data request misses in the cache, first of all, what being contended by Applicant is merely fetching and prefetching of data when cache miss occurs; clearly, as pointed out by Examiner previously, Scales discloses when the requested operand (data) is not in the cache (cache miss); the entired cache line will be filled wherein data size is determined by the size determining logic (column 1, lines 48), and additional operands adjacent in the memory to the requested operand (prefetched data) are also transfer to fill the cache line/entry which clearly (e.g. see column 1, lines 22-57), this clearly meets the argument of transferring multiple data line lengths of data whenever a

data request misses in the cache. Examiner further recognizes that references cannot be arbitrarily combined and that there must be some reason why one skilled in the art would be motivated to make the proposed combination of primary and secondary references. In re Nomiya, 184 USPQ 607 (CCPA 1975). However, there is no requirement that a motivation to make the modification be expressly articulated. The test for combining references is what the combination of disclosures taken as a whole would suggest to one of ordinary skill in the art. In re McLaughlin, 170 USPQ 209 (CCPA 1971). Sachs et al. and Scales III et al. references are evaluated by what they suggest to one versed in the art, rather than by their specific disclosures. In re Bozek, 163 USPQ 545 (CCPA) 1969. In this case, Scales, relied on by Examiner for the utilization of multiple data line lengths of data for cache entry wherein Scales teaches cache memory 22 having a plurality of cache entries wherein each entry can be sized to store multiple data line lengths of data (e.g. see column 7, lines 59 et seq.). In doing so, it would increase the flexibility of Sachs system by allowing it to serve a broader range of applications and their variants; therefore being advantageous. Therefore, the 103 rejection in combining Sachs et al. and Scales III et al. references is deemed to be proper.

10. Applicant's arguments filed February 25, 2002 have been

fully considered but they are not deemed to be persuasive.

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 C.F.R. § 1.136(a).

A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS FINAL ACTION IS SET TO EXPIRE THREE MONTHS FROM THE DATE OF THIS ACTION. IN THE EVENT A FIRST RESPONSE IS FILED WITHIN TWO MONTHS OF THE MAILING DATE OF THIS FINAL ACTION AND THE ADVISORY ACTION IS NOT MAILED UNTIL AFTER THE END OF THE THREE-MONTH SHORTENED STATUTORY PERIOD, THEN THE SHORTENED STATUTORY PERIOD WILL EXPIRE ON THE DATE THE ADVISORY ACTION IS MAILED, AND ANY EXTENSION FEE PURSUANT TO 37 C.F.R. § 1.136(a) WILL BE CALCULATED FROM THE MAILING DATE OF THE ADVISORY ACTION. IN NO EVENT WILL THE STATUTORY PERIOD FOR RESPONSE EXPIRE LATER THAN SIX MONTHS FROM THE DATE OF THIS FINAL ACTION.

12. **Any response to this final action should be mailed to:**

Box AF

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or faxed to:

(703) 308-9051, (for formal communications; please mark "EXPEDITED PROCEDURE")

Or:

(703) 308-6606 (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan V. Thai whose telephone number is 703-305-3842.

The examiner can normally be reached on Monday-Thursday from 6:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor Matthew M. Kim can be reached on (703) 308-3821.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

TVT/June 24, 2002

Tuan V. Thai
PRIMARY EXAMINER
Group 2100